M-12

Improvement of STDP Synaptic Hardware Model for Image Pattern Recognition

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Abstract: Generally, the memory is being maintained by synaptic strength between cell bodies in a hippocampus that take a charge of memory in the brain. STDP (Spike-Timing-Dependent-synaptic-Plasticity) that changes synaptic strength depending on oscillating timing and order of the cell body (PRE) connecting the first part of the synapse and the cell body (POST) connecting the latter part of it is being presumed that it involves memory and learning. We previously proposed a hardware model that can reproduce the STDP characteristics. However, this model has two unfavorable characteristics that the variation of potentiation and depression changes depending on original output electrical potential and output voltage increases slightly in the case of T_{post}-T_{pre} = 0 (T_{post}-T_{pre} means time difference of POST and PRE). In this paper, we propose a STDP synaptic hardware model that improves the above unfavorable characteristics and evaluate circuit characteristics by PVT corner simulation.

1. Introduction

Recently, a study of the modeling of neural network in the human brain is being conducted to apply information processing ability of the human brain to engineering[1]-[3]. These researches provide not only a method that simulates information processing ability of the brain but also unravels calculation principle of the human brain.

Commonly, the memory is being maintained by synaptic strength between two cell bodies in a hippocampus that take a charge of memory and learning in the brain.

STDP (Spike-Timing-Dependent-synaptic-Plasticity)[4] that changes synaptic strength depending on oscillating timing and order of the cell body (PRE) connecting the first part of the synapse and the cell body (POST) connecting the latter part of it is being presumed that it involves memory and learning[1].

We previously proposed a hardware model that can reproduce the STDP characteristics. However, this model has two unfavorable characteristics that the variation of potentiation and depression changes depending on original output electrical potential and output voltage increases slightly in the case of T_{post}-T_{pre} = 0 (T_{post}-T_{pre} means Δt of POST and PRE). In this paper, we propose a STDP synaptic hardware model that improves the above unfavorable characteristics and evaluate circuit characteristics by PVT corner simulation.

2. Methods

Figure 1 shows STDP synaptic hardware model. This model is designated through 0.18μm CMOS process.

Operating principle of STDP synaptic hardware model is described below by division into two cases Tpost-Tpre > 0 and Tpost-Tpre < 0.

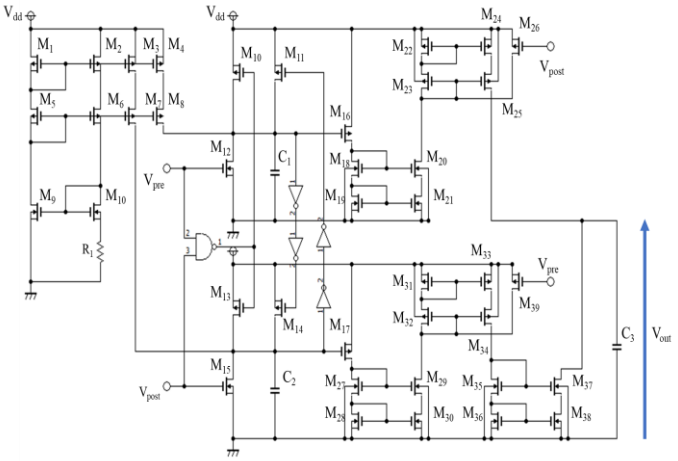

Figure 1. STDP synaptic hardware model

1) T_{post}-T_{pre} > 0

Firstly, when V_{pre} is input, M_{12} is ON and the charge flows from C_1. The gate voltage of M_{16} gradually increases because the current gradually flows from M_4 and M_8 to C_1 at this time. Secondly, M_{16} is ON and cascode current mirror of M_{18}~M_{21} is ON. Nextly, when V_{post} is input, M_{26} is OFF. Thereby cascode current mirror of M_{22}~M_{25} is ON and the charge is supplied to C_3. The bigger time difference is, the more this current flows because amount of this current depends on gate voltage of M_{13}. INV_1 and INV_2 prevent deppression section from operating.

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2) T_{post}-T_{pre} < 0

Firstly, when V_{post} is input, M_{15} is ON and the charge flows from C_2. The gate voltage of M_{17} gradually increases because the current gradually flows from M_3 and M_7 to C_1 at this time. Secondly, M_{17} is ON and cascode current mirror of M_{27}~M_{30} is ON. Nextly, when V_{pre} is input, M_{39} is OFF. Thereby cascode current mirror of M_{31}~M_{38} is ON and the charge flows from C_3. The bigger time difference is, the more this current flows because amount of this current depends on gate voltage of M_{17}. INV_3 and INV_4 prevent potentation section from operating.

Also, AND, M_{12} and M_{15} prevent gate voltage of M_{16} and M_{17} from decreasing.

Figure 2 shows ΔVout vs. Δt characteristics of STDP synaptic hardware model shown in the figure 2. Oscillating frequency of pulse waves input to PRE and POST are 20kHz. Time difference is changed from -15μs to 15μs including 0μs. From simulation results, V_{out} shown vertical axis is positive provided that T_{post}-T_{pre} is positive and it is nagative provided that T_{post}-T_{pre} is negative. As time difference shown horizontal axis becomes shorter, the amplitude increases. Also, this figure shows V_{out} don't change in the case of time difference is 0μs.

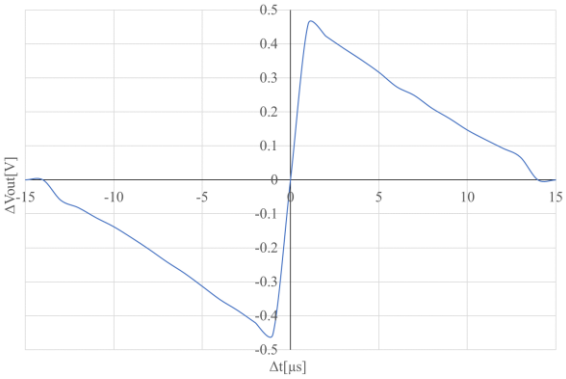

Figure 2. Δ_t vs. ΔV_{out} characteristics of STDP synaptic hardware model

Figure 3 shows MOSFETs characteristics of STDP synaptic hardware model. The 5 patterns changed MOSFETs characteristics are shown below:

1. N channel MOSFETs are typical device model and P channel MOSFETs are typical device model (NTPT).
2. N channel MOSFETs are slow device model and P channel MOSFETs are slow device model (NSPS).
3. N channel MOSFETs are fast device model and P channel MOSFETs are slow device model (NFPS).
4. N channel MOSFETs are fast device model and P channel MOSFETs are fast device model (NFPF).
5. N channel MOSFETs are slow device model and P channel MOSFETs are fast device model (NSPF).

Output voltage is very low and 0 provided NFPF and NFPS because the amperage that flows from current source to C_1 and C_2 increases by changing M_9 and M_{10} into fast device.

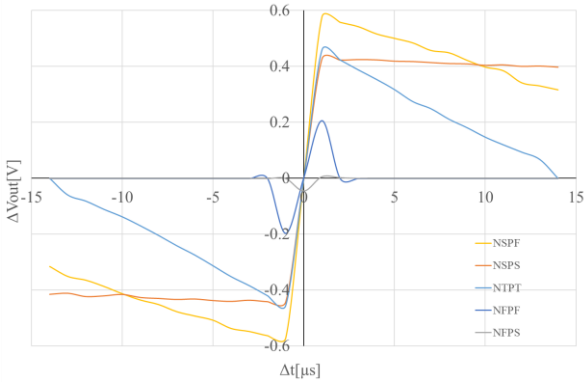

Figure 3. MOSFETs variation characteristics of STDP synaptic hardware model

3. Conclusion

In this paper, we improved STDP synaptic hardware model for image pattern recognition and evaluated characteristics of this circuit by using the PVT corner condition.

In future work, we will actually apply this circuit to image pattern recognition and define evaluation index of PVT variation considering effect that the neural network system this circuit is operated will cause. Thereafter we will construct an IC chip based the considering effect for the PVT variation.

4. References

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